DATA TEST INTERFACE (DTI), 628458

GENERAL DESCRIPTION

CONTENTS PAGE

1. GENERAL 1
2. DESCRIPTION 1
3. FUNCTIONAL OPERATION (FIG. 2) 1
4. OPTIONS 2
5. TEST AND MAINTENANCE FEATURES 2
6. TECHNICAL SUMMARY 2
7. REFERENCES 2

1. GENERAL

1.01 This Section provides a general description of the ITT D448 data test interface (DTI), 628458 (Fig. 1), to the functional block diagram level.

1.02 Whenever this Section is reissued, the reasons for reissue will be listed in this paragraph.

TO BE SUPPLIED

Fig. 1—DTI, 628458

1.03 The DTI is an accessory piece of test equipment used to interface data test sets with the D448 dataport system clock for dataport testing. Both a 64-kHz bit clock and an 8-kHz byte clock are provided to the test sets. Since the DTI only extracts timing for testing purposes, it may be installed or removed from the system without affecting system performance.

Note: The DTI is designed to be used with the data test sets listed in Section ITTR-18-600.

2. DESCRIPTION

2.01 The unit mounts in the D448 multiplex shelf (common equipment section) in the DTI connector position. Installation procedures for the unit may be found in Section ITTR-18-442.

2.02 The unit is available in Group -001 only.

2.03 The unit consists of an epoxy-glass printed circuit board (PCB); a sheet metal closure which provides mounting space for two 5-pin audio connectors (J1, J2) and an extraction handle and also protects the unit electronic components; and associated components. The unit name, part number, and issue letter are also located on both the closure side and the component side of the PCB.

2.04 Printed circuit wiring is etched on both sides of the PCB. Unit inputs and outputs are terminated in gold-plated contacts on the rear edge of the PCB. These contacts mate with a 70-pin contact edge connector on the rear of the multiplex shelf.

3. FUNCTIONAL OPERATION (FIG. 2)

3.01 The DTI uses two clock inputs. These are the BIT and BYTE clocks from the office interface unit/DDS (OIU/DDS). Both clocks initially are TTL levels referenced to $-5V$.

3.02 The 64-kHz BIT clock enters the DTI on pin 4 of the card edge connector. The DTI bit clock circuit buffers the input BIT clock and level-shifts it from the $-5V$ system voltage to the $+5V$ required by the data test sets. The bit clock circuit produces two outputs: the level-shifted 64-kHz BIT clock and an inverse 64-kHz clock ($\overline{\text{BIT}}$). These outputs are sent to the TO XMTR and TO RCVR jacks (J1 and J2, respectively) on the DTI front panel.

3.03 The 8-kHz BYTE clock enters the DTI on pin 7 of the card edge connector. The DTI byte clock circuit reclocks the 8-kHz BYTE clock (to remove glitches) and level-shifts it from the $-5V$ system voltage to the $+5V$

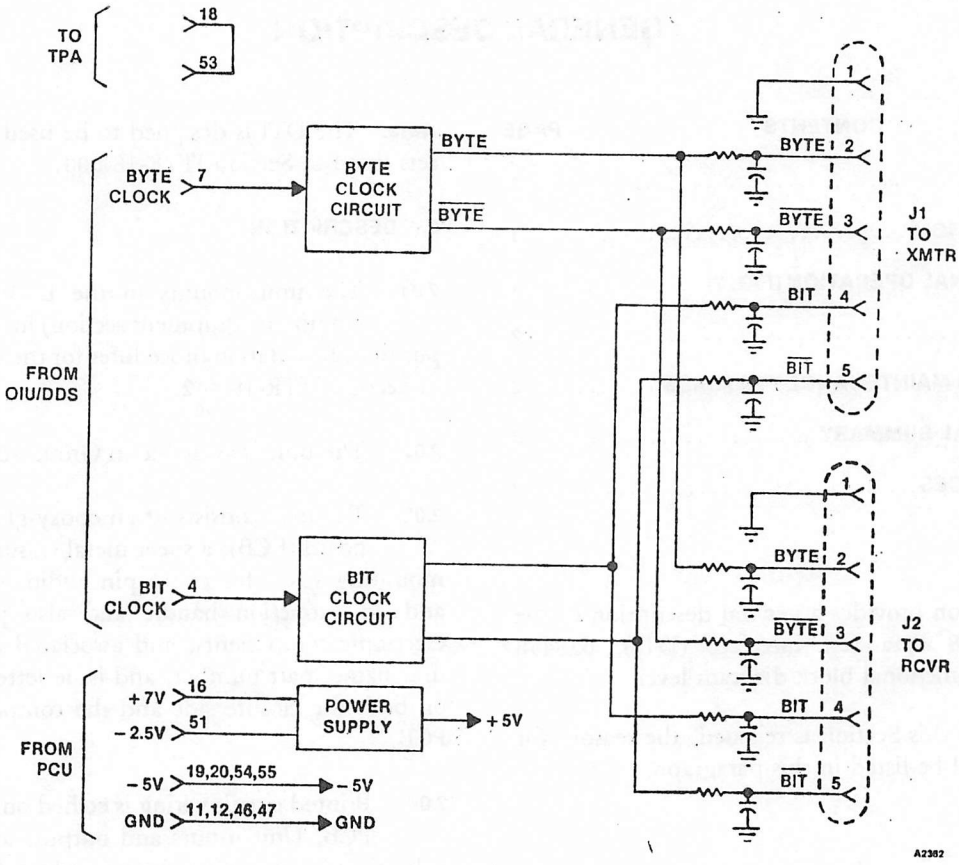

Fig. 2—DTI, 628458, Functional Block Diagram

required by the data test sets. The byte clock circuit produces two outputs: the level-shifted 8-kHz BYTE clock and an inverse 8-kHz clock ($\overline{\text{BYTE}}$). These outputs are sent to the TO XMTR and TO RCVR jacks on the DTI front panel.

3.04 The power supply uses +7V and −2.5V system voltages to produce the +5V required for the output signals.

4. OPTIONS

4.01 The unit has no field-selectable options.

5. TEST AND MAINTENANCE FEATURES

5.01 A description of the test and maintenance features on the unit is provided in Table A. Refer to Fig. 1 for the physical location of these features.

TABLE A

FEATURE	REF. DES.	FUNCTION
TO XMTR Jack	J1	Provides access to data test transmitter.
TO RCVR Jack	J2	Provides access to data test receiver.

6. TECHNICAL SUMMARY

6.01 A summary of the technical specifications of the unit is given in Table B.

7. REFERENCES

7.01 The engineering drawings noted in Table C were used in the preparation of this Section.

TABLE B

ITEM	SPECIFICATION
INPUT POWER REQUIREMENTS	
Voltage	+7.0 ±0.6 Vdc; −5 ±0.25 Vdc; +2.5 ±0.005 Vdc
Current (Maximum)	50 mA @ 7V; 35 mA @ −5V; 50 uA @ 2.5V
OPERATING ENVIRONMENT	
Temperature	0° to 55°C
Humidity	To 95% at 40°C (no condensation)
Altitude	To 14,000 ft (4,300 m)
DIMENSIONS	
Height	5.0 in. (12.7 cm)
Width	1.0 in. (2.5 cm)
Depth	9.6 in.(24.4 cm)
WEIGHT	0.8 lb (0.4 kg)

TABLE C

TYPE	DRAWING NO.
Assembly	628458-000
Schematic	628458-002

7.02 Related information on the unit may be found in the ITTR Sections referenced in Table D.

TABLE D

TITLE	SECTION NO.
Dataport Channel Units — Option Selection and Installation	ITTR-18-442
D448 PCM Trunk Carrier System — Recommended Test Equipment	ITTR-18-600